## REMARKS

Reconsideration of this application is requested. Claims 18, 20, 23, 31, 33, 41 and 45 to 49 are pending. The pending independent claims are 18 and 49.

The objections to the claims have been overcome by amending claims 18, 23 and 46 in the manner suggested in the Action. These amendments are not being made to distinguish prior art.

Claim 18 has been amended to make clear that the source enable signal is generated by a source enable signal output circuit, and that the source enable signal is at a selecting level. This amendment is supported by the original application at page 40, lines 9 to 13 and by Figure 25. The power source control circuit 81 is an exemplary source enable signal output circuit, and outputs a source enable signal to the source enable signal line 70 connected to the source driver control circuit 54.

Regarding the PTO's comments stated in paragraph 5 of the Advisory Action:

- With respect to comment (i), claim 18 does recite a "source driver", a "source driver control circuit", and now a "source enable signal output circuit", but these circuit elements are not disclosed in Yasui in the manner being claimed herein;
- With respect to comment (ii), claim 18 has been amended to make clear that when the source enable signal causes the source driver control circuit,

to command the power maintaining means to apply an OFF voltage to the pixel electrodes, and

- With respect to comment (iii), claim 18 has been amended to make clear that the source driver control circuit does cause the OFF voltages to be applied to the pixel electrodes.

As each of the specific comments made in the Advisory Action have been addressed and the rejection overcome, claim 18 should be in clear condition for allowance. The Advisory Action did not provide any details regarding the rejection of claim 46 and, thus, that rejection should be withdrawn for reasons previously stated.

The rejection of claims 18, 20, 23, 41 and 45 to 49 as being anticipated by Yasui et al (US Patent 5,248,963 -- Yasui) is traversed.

Independent claims 18 and 49 recite an LCD erasing device that applies a signal to the electrodes for the pixels after the LCD power is turned off. In particular, claim 18 recites that a "source enable signal output circuit" generates a "source enable signal" that is "at a selecting level during the certain period [which is a period following power being turned off, and the selecting level] is inputted into said source driver circuit so that said pixel electrode and said opposing electrode receive an OFF voltage that turns OFF a liquid crystal." *See, e.g.*, Appln. pp. 39-49 (emphasis applied).

Yasui discloses supplying a common potential to both a display electrode 12a and a counter electrode 12b within a time (T) after the power is turned OFF (see column 6, lines 3 to 6). Yasui discloses that pixel data (D) is set to a logic "0" to clear the display.

Yasui, col. 3, lns. 59-61. The pixel data is loaded into a shift register and then applied to the pixels. Yasui does not disclose a feature in which "source enable signal output circuit" generates a "source enable signal" that is inputted to the source driver control circuit during a predetermined period after the power source is turned OFF.

The Action mischaracterizes Yasui with respect to the power holding circuit 22 and power circuit 23 which apply a post-OFF voltage to the gate bus drive circuit 17, rather than the source bus drive circuit 16. *See* Yasui, col. 4, lns. 59-64. Contrary to the Action, the power holding circuit 22 and power circuit 23 and associated capacitor 25 and inverter 27 (not identified in drawings) relate to the gate bus drive circuit 17 and not to the source bus drive circuit 16. The Action states that a capacitor (25), a resistor (26), an inverter (27), and a voltage $V_B$ correspond to the source driver control circuit, and the source enable signal respectively. However, Yasui Fig. 5 and the descriptions in column 5, lines 8 to 53, make clear that these elements are provided for supplying a voltage $V_{CL}$ to a gate bus driver circuit 17, and have nothing to do with a source bus driver circuit 16. Yasui teaches that a post-OFF signal high-level output voltage ($V_{CL}$) is applied to cause the gate bus driver 17. Yasui, col. 5, lns. 31-64). The $V_{CL}$ high-level output voltage causes the TFTs for each pixel to be turned ON such that the source bus driver 16b to apply a common potential to the display electrodes. Yasui, col. 5, ln. 59 to col. 6, ln. 11.

The source of the source control signals (D, PCK, and M) for the source bus drive circuit is not disclosed in Yasui. Even assuming that there must be a signal source for supplying to source bus circuit 16 the D, PCK and M signals, Yasui does not disclose a

source enable signal output circuit for supplying a source enable signal to a source driver control circuit to cause the source driver to have an OFF voltage applied to the pixel electrodes.

Unlike Yasui, claim 18 herein recites that a source enable signal is inputted to the "source" driver control circuit at a "selection level" during the predetermined period after the power source is turned OFF. Such use of the "source" enable signal does not complicate the circuit arrangement and allows application to the pixel electrode and the opposing electrode, a voltage for turning OFF the liquid crystal. Because Yasui teaches display erasing by means, (e.g., gate control and loading "O" into source driver) other than a source enable signal, it teaches away from the invention recited in claim 18

Claims 45 and 49 recite "rectangular wave signals" being applied by the LCD erasing means. In particular, claim 49 recites that the erasing means "applies rectangular wave signals, identical in terms of phase and potential, respectively into said pixel electrode and said opposing electrode during the certain period" which follows the power source being turned off. *Id.* In contrast to claim 49, Yasui discloses applying a constant common (ground) potential to both the display electrode 12a and the counter electrode 12b within the time T after the power is turned OFF (see column 6, lines 3 to 6). Yasui (column 1, line 52) states " common potential EG (zero volt", the "common potential EG" is the ground potential.

Yasui teaches that a ground potential EG is supplied to both the display electrode 12a and the counter electrode 12b within the time T after the power is turned OFF. Yasui

(column 5, line 6, to column 6, line 1) describes that "[t]he source bus driver 16b is arranged so that the potential as its output terminal goes to the common potential EG at substantially the same time as the operating voltages $E_1$, $E_2$ and $E_3$ drop to the common potential". Yasui discloses in column 6, lines 3 to 6 that a common potential is supplied to a display electrode 12a and an opposing electrode 12b (a DC voltage $E_2$ is supplied to the opposing voltage 12b) within a time (T) after the power is turned OFF. The above parenthetic disclosure of Yasui merely teaches that within a certain period (T), the voltage E2 is supplied to the opposing electrode 12b. Yasui fails to disclose or suggest the structure of supplying the voltage $E_2$ after an elapse of certain time (T) after the power source is turned OFF. Yasui fails to disclose or suggest the structure of supplying the voltage $E_2$ after supplying the ground potential EG.

The Action incorrectly characterizes Yasui as disclosing at column 6, lns. 1-11 (see also column 3, line 58 to column 4, line 16), that a DC voltage ($E_2$ and common) I supplied to the display electrodes 12a and 12b by the source buses 14t through $14_1$ through $14_n$ to clear the display. Yasui (column 1, lines 45 to 60) states that the $E_2$ is a DC voltage. This description in Yasui indicates that a DC voltage is supplied to both the display electrode 12a and the counter electrode 12b within the time T after the power is turned OFF.

Yasui does not disclose the rectangular wave signals, recited in claim 49, that are identical in terms of phase and potential, respectively into said pixel electrode and the opposing electrode. Yasui states that during the certain time (T) after the power source is

turned OFF, a constant common potential (EG or $E_2$) is supplied to the display electrode 12a and the opposing electrode 12b. Yasui fails to disclose the structure wherein rectangular wave signals that are identical in terms of phase and potential are supplied to the display electrode and the opposing electrode.

The rejection of claims 31 and 33 for obviousness over Yasui is traversed for the reasons stated above for claims 18.

All claims are in good condition for allowance. If any small matter remains outstanding, the Examiner is requested to telephone the undersigned. Prompt reconsideration and allowance of this application is requested.

Respectfully submitted,

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